Topic: 1.3.2 Computer architecture and the fetch execute cycle

Von Neumann Architecture:

1. (a) Describe what is meant by Von Neumann architecture. **[3]**
   (b) Explain the purpose of each of the following special registers in a processor.
   (i) Program Counter (Sequence Control Register). **[2]**
   (ii) Current Instruction Register. **[2]**
   (iii) Memory Address Register. **[2]**
   (iv) Memory Data Register. **[2]**
   (v) Accumulator

2. (a) Describe the purpose of the following registers in a processor:
   (i) Current instruction register (CIR), **[2]**
   (ii) Memory address register (MAR), **[2]**
   (iii) Program counter (PC), **[2]**
   (iv) Index register (IR). **[2]**

3. (a) Describe what is meant by Von Neumann architecture. **[2]**

4. (a) State the purpose of the Memory Address Register (MAR) in a computer. **[1]**
   (b) Describe two stages of the fetch/execute cycle which would change the contents of the MAR. State clearly, in each case, what the MAR contains. **[4]**

5. (a) (i) State what is held in the Program Counter (PC) during the fetch /execute cycle. **[1]**
   (ii) Explain how the contents of the PC change during the fetch/execute cycle. **[4]**
   (b) Describe the contents of the memory address register (MAR) during the fetch/execute cycle. **[4]**

9. (a) Describe basic Von Neumann processor architecture. **[3]**
   (b) At a particular point in a program, the program counter (PC) contains the value 200.
   (i) State the expected value contained in the PC after the instruction held at location 200 has been fetched.

Explain your answer. **[2]**

(ii) After the instruction is processed, the value in the PC is 180.

Explain why the value has changed to 180. **[2]**

10. State what is stored in each of the following special purpose registers in a computer and explain how the contents are altered during the fetch/execute cycle.

(i) MAR **[3]**

(ii) MDR (or MBR) **[3]**

(ii) CIR **[3]**

11. (a) Explain what is meant by Von Neumann architecture. **[3]**

(b) (i) Explain what the accumulator holds and how the contents change during the fetch-execute cycle. **[2]**

(ii) Explain what the program counter (PC) holds and how the contents change during the fetch-execute cycle. **[3]**

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7 (a) One of the key features of von Neumann computer architecture is the use of buses.
Three buses and three descriptions are shown below.
Draw a line to connect each bus to its correct description.

Bus	Description
address bus	this bus carries signals used to coordinate the computer's activities
control bus	this bi-directional bus is used to exchange data between processor, memory and input/ output devices
data bus	this uni-directional bus carries signals relating to memory addresses between processor and memory

[2]

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(b) The seven stages in a von Neumann fetch-execute cycle are shown in the table below.
Put each stage in the correct sequence by writing the numbers 1 to 7 in the right hand column.
The first one has been done for you.

Stage	Sequence number
the instruction is then copied from the memory location contained in the MAR (memory address register) and is placed in the MDR (memory data register)	
the instruction is finally decoded and is then executed	
the PC (program counter) contains the address of the next instruction to be fetched	**1**
the entire instruction is then copied from the MDR (memory data register) and placed in the CIR (current instruction register)	
the address contained in the PC (program counter) is copied to the MAR (memory address register) via the address bus	
the address part of the instruction, if any, is placed in the MAR (memory address register)	
the value in the PC (program counter) is then incremented so that it points to the next instruction to be fetched	

[6]